Area and Power Efficient VLSI Architecture for FIR Filter using Asynchronous Multiplier

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Abstract

The FIR filter is commonly used in many applications such as communication or multimedia signal processing. In the existing method, the design of FIR filter structure, based on synchronous multiplier such as Wallace tree multiplier design is considered. It leads to fewer throughputs and increase in hardware complexity but there is considerable decrease in power consumption. This paper is focused on the design of an efficient VLSI architecture for asynchronous multiplier based FIR filter design which aims at reducing the power and area. The proposed FIR filter design is based on low-voltage micro power asynchronous signed truncated multiplier which corresponds to shift-add multiplication approach .The emphases of the design are micro power operation and small IC area and high throughput, and these attributes are achieved in several ways.

Keywords: FIR filter, Wallace tree multiplier, Asynchronous multiplier, Shift-add multiplication approach.

1. Introduction

Modern DSP systems are well suited for VLSI implementation .Indeed, they are often technically feasible or economically viable only if implemented using VLSI technologies.Many DSP systems are produced in very large numbers and require high performance circuits with respect to throughput and power consumption.

The combined advances in system design capability and VLSI technology have made it possible to economically design unique integrated circuits or use in dedicated applications, so called Application Specific Integrated Circuits (ASIC).The possibility of incorporating a whole signal processing system into an chip has multitude of effects. It will dramatically increase the processing capacity and simultaneously reduce the size of the system, the power consumption.

In the existing method, the design of FIR filter structure, based on synchronous multiplier such as Wallace tree multiplier design is considered.. It leads to fewer throughputs and increase in hardware complexity but there is considerable decrease in power consumption. This paper is focused on the design of an efficient VLSI architecture for asynchronous multiplier based FIR filter design which aims at reducing the power and also to increase the computation speed. The proposed FIR filter design is based on low-voltage micro power asynchronous signed truncated multiplier which corresponds to shift-add multiplication approach .The emphases of the design are micro power operation and small IC area and high throughput, and these attributes are achieved in several ways. By employing an signed magnitude data representation, there is less power-wasting switching activities. A low power transmission gate shifter

structure is adopted. The partial products are truncated to obtain a fixed 16-bit signed product, thereby reducing 50% of hardware. Latch adder is employed, it features an adder with an integrated latch, which dissipates less power and occupies less IC area than the usual independent adder and independent latch. A transparent (T-latch) is proposed and used to block unnecessary switching. And a novel power-efficient speculative delay line is used to control the asynchronous operation. The error arising from truncation is analyzed.

By comparing the synchronous multiplier and asynchronous multiplier, the asynchronous multiplier has low power dissipation with lesser area consumption. Because of low power dissipation and less area consumption, the FIR filter can be designed using asynchronous multiplier.

2. Previous Research

Shahnam Mirzaei et al suggested that the method for implementing high speed Finite Impulse Response using just registered adders and hardwired shifts. Modified common sub expression elimination algorithm was used to reduce the number of adders in this paper. There is a 50% reduction in number of slices and 75%reduction in number of LUTs for fully parallel implementations. There is a 50% reduction in the total dynamic power consumption of the filters. This design performs significantly faster than MAC filters, which uses embedded multipliers.

D.L.Maskell et.al suggested that the algorithm for reducing the hardware complexity of linear phase finite impulse response digital filters that minimize the adder depth block adders in the Multiplier Block Adders. The algorithm is used for reducing both the coefficient word length and the number of non-zero bits in the filter coefficients. This reduces the number of adders that are needed to construct the coefficient multiplier and results in an increased operating frequency. Discrete coefficient optimization techniques based on mixed integer linear programming using minimum normalized peak ripple magnitude was proposed. Common Sub expression Elimination attempt to minimize the number of additions in the multiplier block by combining signed digit terms.

Common Sub expression Elimination algorithm is used for reducing the hardware complexity of linear phase FIR digital filters without increasing the adder depth in the MBAs. In fact, to reduce the number of non-zero bits in the filter coefficients adder depth can be reduced was attempted. A modification was also proposed to the representation of the filter coefficients such that the number of FAs in our hardware implementation is proportional to only the product of signal word length and the number of adders. Result shows that there is 70% reduction in number of MBAs and the number of FAs respectively.

Thomas Poonnen et al introduced that the design of FIR filter is based on an existing parameterized divide and conquer algorithm that uses optimal partioning and redundancy removal for simultaneous computation of partial sums. The VLSI implementation of the proposed Parameterized Binary multiplier architecture is obtained by applying this algorithm to the iterative array multiplier implementation. Two variations of the PBMA, namely PBMA-A and PBMA-AT are implemented and compared to the conventional carry save Array multiplier. The iterative array multiplier architecture is preferred over faster tree architectures like Wallace multiplier or the dada multiplier. However, as the width of multiplicand or the multiplier increases there is a corresponding increase in the width or the number of required partial products making it unsuitable for arithmetic intensive applications such as signal processing, scientific computations and cryptography.

Thus for ultra low-power applications, it is recommended to derive a power optimized VLSI implementation scheme for the PBMA from low power components. This may compromise some of the

area or operational delay savings, but is more desirable for portable applications with power consumption are a major issue.

A.P.Vinod et al suggested a method called Minimal-difference differential coefficients method which was presented for low power and high speed realization of differential-coefficients-based finite impulse response filters. The conventional differential coefficients method (DCM) uses the difference between adjacent coefficients whereas the coefficients that have the least difference between their magnitude values were identified.

Minimal-difference differential coefficients method can be coded using fewer bits, which in turn reduces the number of full additions required for coefficient multiplication. By employing a differential – coefficient partitioning algorithm and a pseudo floating-point representation it was shown that the number of full adders and net memory needed to implement the coefficient multipliers can be significantly reduced. The proposed method is combined with Common Subexpression elimination for further reduction of complexity .Experimental result shows the average reductions of full adder, memory and energy dissipated achieved by this method over the DCM is 50%.

3. **Overview of the Existing System**

A digital finite impulse response(FIR) filter performs the frequency shaping or the linear prediction on a discrete-time input sequence$\{X_0,X_1,X_2\ldots\ldots\}$.This project is focused on the design of an efficient VLSI architecture for asynchronous multiplier based FIR filter design which aims at reducing the power and also to increase the computation speed.

In the proposed asynchronous multiplier 16x16 asynchronous shift-add multiplier is used, whose critical parameters include low-voltage (1.1V) micro power (5.86micro watts at 1MHz, 0.35 micro metre CMOS) operation and a small IC area. The proposed multiplier handles up to three signed power-of-two(SPT) terms and is unique as it utilizes a sign magnitude(SM) data representation(as opposed to two's complement).By handling three SPT terms, the proposed design is less restricted than several reported designs. Micro power operation is achieved in several ways.

By employing an SM data representation, there is less power-wasting switching activities. A low power transmission gate shifter structure is adopted. The partial products are truncated to obtain a fixed 16-bit signed product, thereby reducing 50% of hardware. Latch adder is employed, it features an adder with an integrated latch, it dissipates less power and occupies less IC area than the usual independent adder and independent latch.

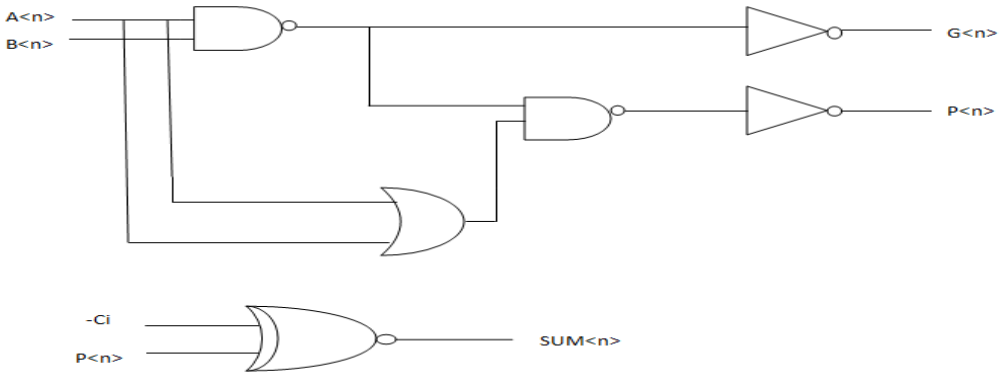
A transparent (T-latch) is proposed and used to block unnecessary switching. A novel power-efficient speculative delay line is proposed that controls the asynchronous operation. The error arising from truncation is analyzed.

3.1 Adder(Manchester Carry Adder):

Manchester carry architecture with a dynamic adder provides improved generate function control as shown in Figure. A 4-bit adder can be constructed by cascading four such stages and constructing the circuitry to supply the appropriate signals. This is commonly called a Manchester carry adder.. However, the intermediate carry gates are no longer needed since the carry values are available in a

distributed fashion. As further shown in Figure 1, if all propagate signals are true, and C is high, six series N-channel transistors pull the output node down. Thus, the worst-case propagation time can be improved by by passing the four stages if all carry propagate signals are true.

Figure 1: Manchester Carry Adder



3.2 Multipliers

Multiplication is one of the most frequently encountered arithmetic operations in floating point processors and digital signal processing applications such as digital filtering, DCT, FFT, CDMA and many others. To increase the speed of computation, digital multipliers are usually implemented in hardware that generates all bit products and sums in parallel using an array or tree of adding elements. These parallel multipliers are fast but need a large number of transistors, resulting in significant power consumption.

3.2.1 Wallace Tree Multiplier

A Wallace tree multiplier is an efficient implementation of a digital circuit that multiplies two integers.

The Wallace tree has three steps:

i)Multiply (AND operation) each bit of one of the arguments, by each bit of the other, yielding n^2 results. Depending on position of the multiplied bits, the wires carry different weights, for example wire of bit carrying result of a_2b_3 is 32 .

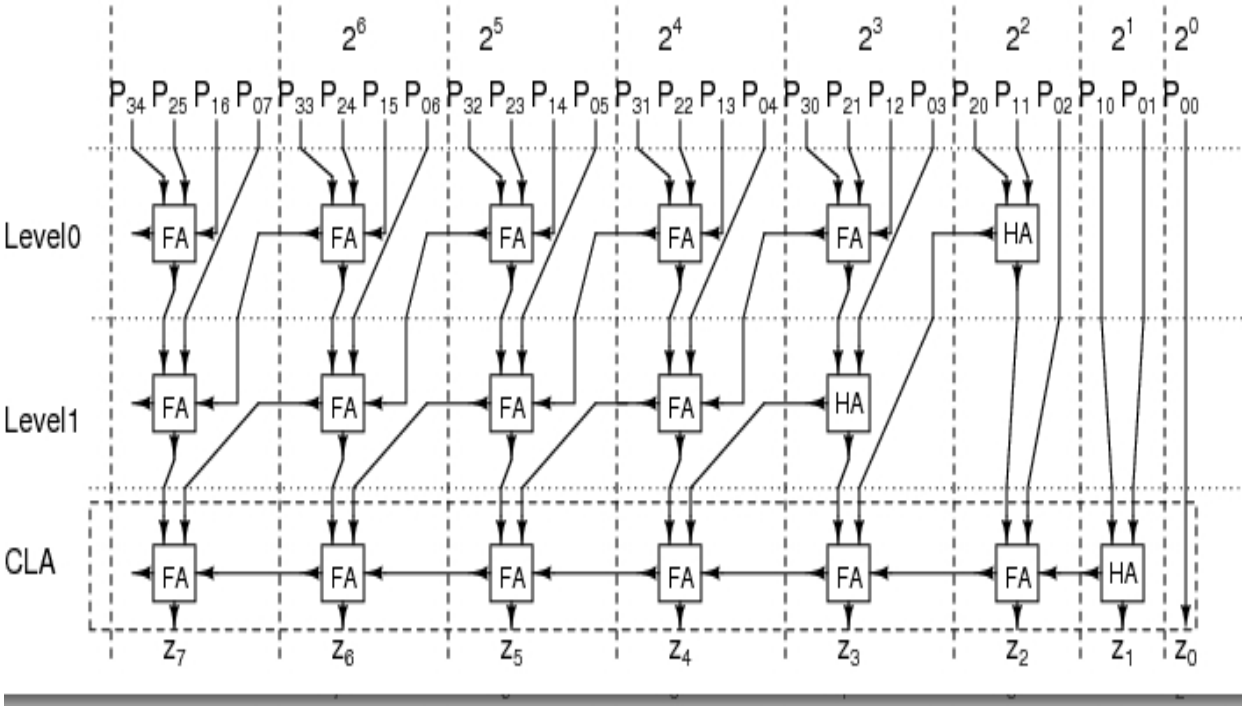
ii) Reduce the number of partial products to two by layers of full and half adders.

iii) Group the wires in two numbers, and then add them with a conventional adder

3.2.2 Architecture of 4x4 Wallace Tree Multiplier

Wallace's strategy is to combine the partial product bits at the earliest opportunity, which leads to the fastest possible design. The Figure 2 shows the architecture of 4x4 Wallace Tree Multiplier.

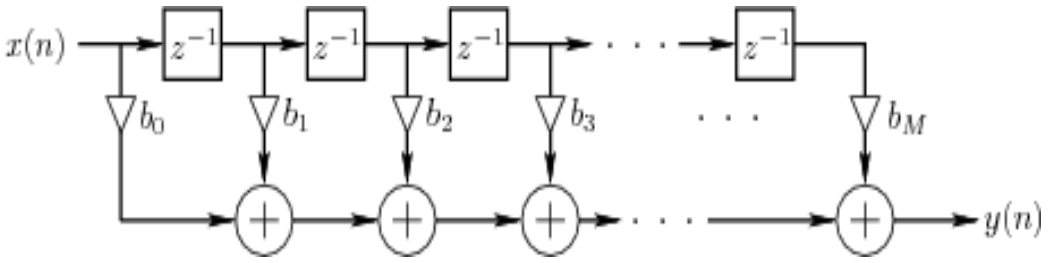
Figure 2: Architecture of 4X4 Wallace Tree multiplier



4. Proposed System

A digital finite impulse response(FIR) filter performs the frequency shaping or the linear prediction on a discrete-time input sequence{X_0,X_1,X_2…….}.This project is focused on the design of an efficient VLSI architecture for asynchronous multiplier based FIR filter design which aims at reducing the power and also to increase the computation speed.

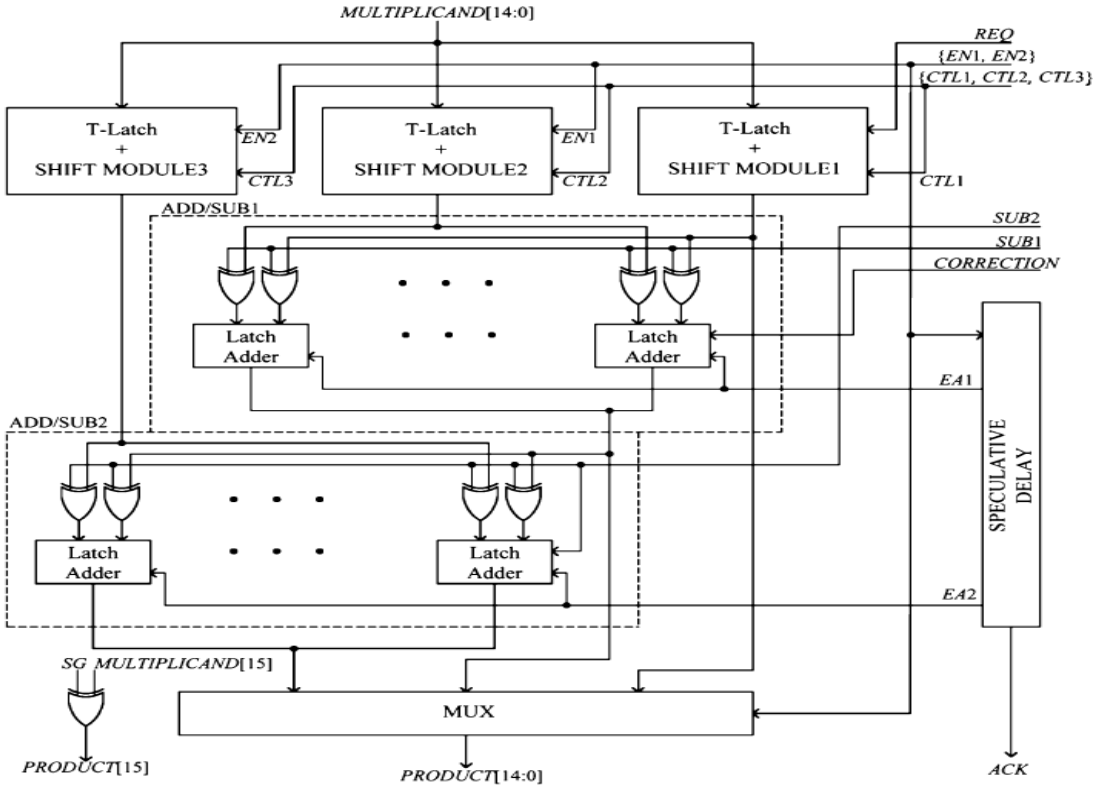
Figure 3: Direct Form FIR



In the proposed FIR filter design, asynchronous multiplier is used which is shown in Figure 4, 16*16 asynchronous shift-add multiplier is used, whose critical parameters include low-voltage (1.1V) micro power (5.86micro watts at 1MHz, 0.35 micro metre.CMOS) operation and a small IC area. The proposed multiplier handles up to three signed power-of-two(SPT) terms and is unique as it utilizes a sign magnitude(SM) data representation(as opposed to two's complement).By handling three SPT terms, the proposed design is less restricted than several reported designs. Micro power operation is achieved in several ways.

By employing an SM data representation, there is less power-wasting switching activities. A low power transmission gate shifter structure is adopted. The partial products are truncated to obtain a fixed 16-bit signed product, there by reducing 50% of hardware. Latch adder is employed, it features an adder with an integrated latch,which dissipates less power and occupies less IC area than the usual independent adder and independent latch . A transparent (T-latch) is proposed and used to block unnecessary switching. And a novel power-efficient speculative delay line is used to control the asynchronous operation. The error arising from truncation is analyzed.

Figure 4: Architecture for Asynchronous Multiplier with Shift-Add Multiplication Approach



The proposed multiplier handles three signed power of two terms and is unique as it utilizes a sign magnitude data representation .The inputs are the multiplicand operands and the control signals are REQ(to initiate multiplication).EN1,the enable signal is given, the second SPT term exists thereby enabling the processing of second SPT term.EN2,the third SPT term exists and thereby enabling the processing of third SPT term.CTL1 is used to control the shift operation of SHIFT MODULE1, CTL2 is used to control the shift operation of SHIFT MODULE2 and CTL3 is used to control the shift operation of SHIFT MODULE3.When the second SPT term is negative, the subtraction operation is performed in ADD/SUB1 module by enabling the signal SUB1.In similar manner when the third SPT term is negative the subtraction operation is performed in ADD/SUB2 module by enabling the signal SUB2.The outputs are PRODUCT and ACK. Acknowledgement signal is given for the indication of multiplication.

The multiplier operand can be predecoded and stored directly as control signals rather than actual 16 bit coefficients in memory. Decoding circuit hardware is not required in this multiplier circuit. The approach results in simpler hardware as there is no need to convert the coefficients to control signals. The asynchronous approach adopted in the multiplier for simplicity and for low power dissipation. The asynchronous approach is attributed for because it is a self-timed circuit with inherent timing control. The latch adder therein controlled adaptively by a novel speculative delay line to control the asynchronous multiplier. Additional latch is not required to store the intermediate results .By means of asynchronous operation, the multiplier operates such that the only modules that are necessary for multiplication process are enabled and the remaining modules are disabled, thereby blocking unnecessary switching. The overall hardware is simple comprising only three shift modules with a T-latch at the input two Latch adders/Subtractors.

5. Results and Discussion

The designed synchronous Wallace tree multiplier reduces power but it occupies larger area, in order to reduce area and also power Low-Voltage Micro power Asynchronous multiplier with Shift-Add Multiplication Approach is simulated.

5.1 Half Adder:

Simulation of half adder is shown in Figure[5]. The inputs are a_i and b_i, and the outputs are s and c. When a_i=1 and b_i=0 and the corresponding outputs are sum=1 and carry=0.

Figure 5: Simulation of Half Adder

5.2 Full Adder:

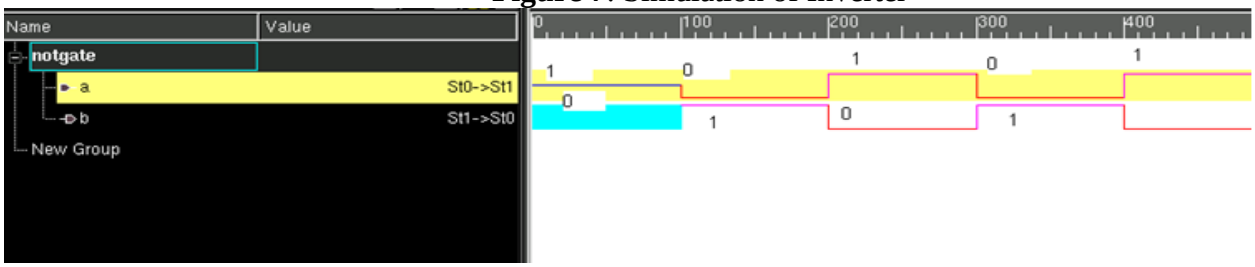
Simulation result of full adder is shown in Figure [6] a, b and c are inputs. S and CY are outputs. When a, b and c are 0 we get sum=0 and carry=0.

Figure 6: Simulation of Full Adder

5.3 Inverter:

Simulation result of inverter is shown in Figure [7]. When a=1 we get the output b as 0 and vice versa.

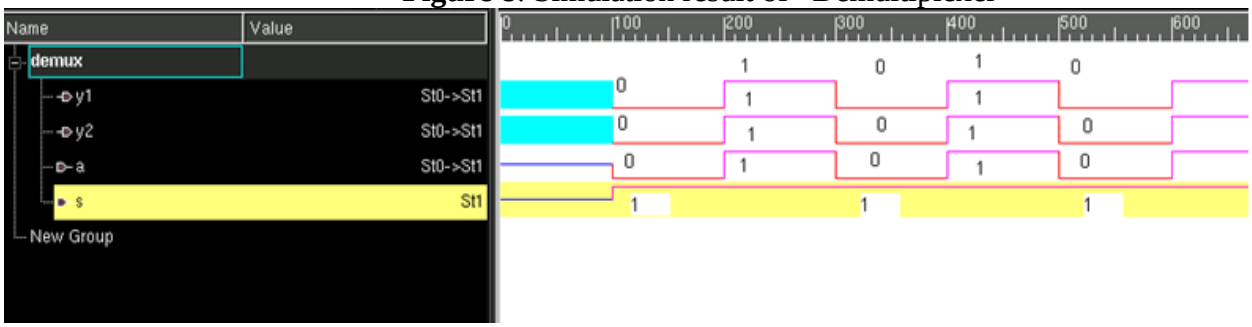
Figure 7: Simulation of Inverter



5.4 Demultiplexer:

Simulation result of demultiplexer is shown in Figure [8]. S is the selection line.y1 and y2 are inputs, thus when both are 0.We get the output a as 0.

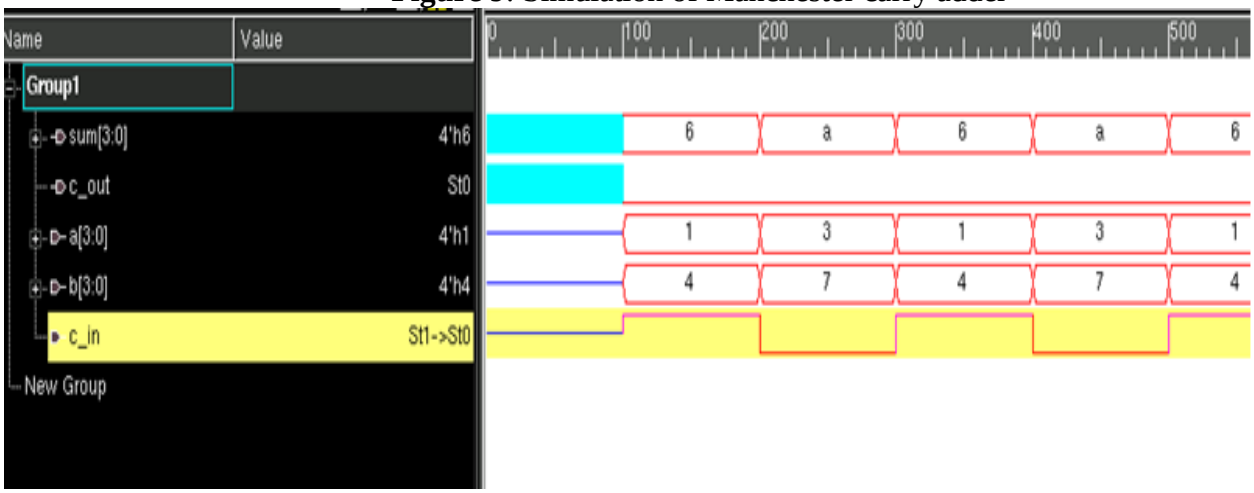
Figure 8: Simulation result of Demultiplexer



5.5 Manchester Carry Adder:

Simulation result of Manchester carry adder is shown in Figure [9] when a is 7, b is 3 and Cin is 0 we get the sum as 10 (hexadecimal “a”).

Figure 9: Simulation of Manchester carry adder



5.6 **(8x8) Wallace Tree Multiplier:**

The simulation result of Wallace Tree multiplier is shown in Figure [10], the multiplier value is 10010(octal-22) and the multiplicand value is 11110001(octal-361), and the final product obtained as 1000011110010.

Figure 10: Simulation of Wallace Tree Multiplier

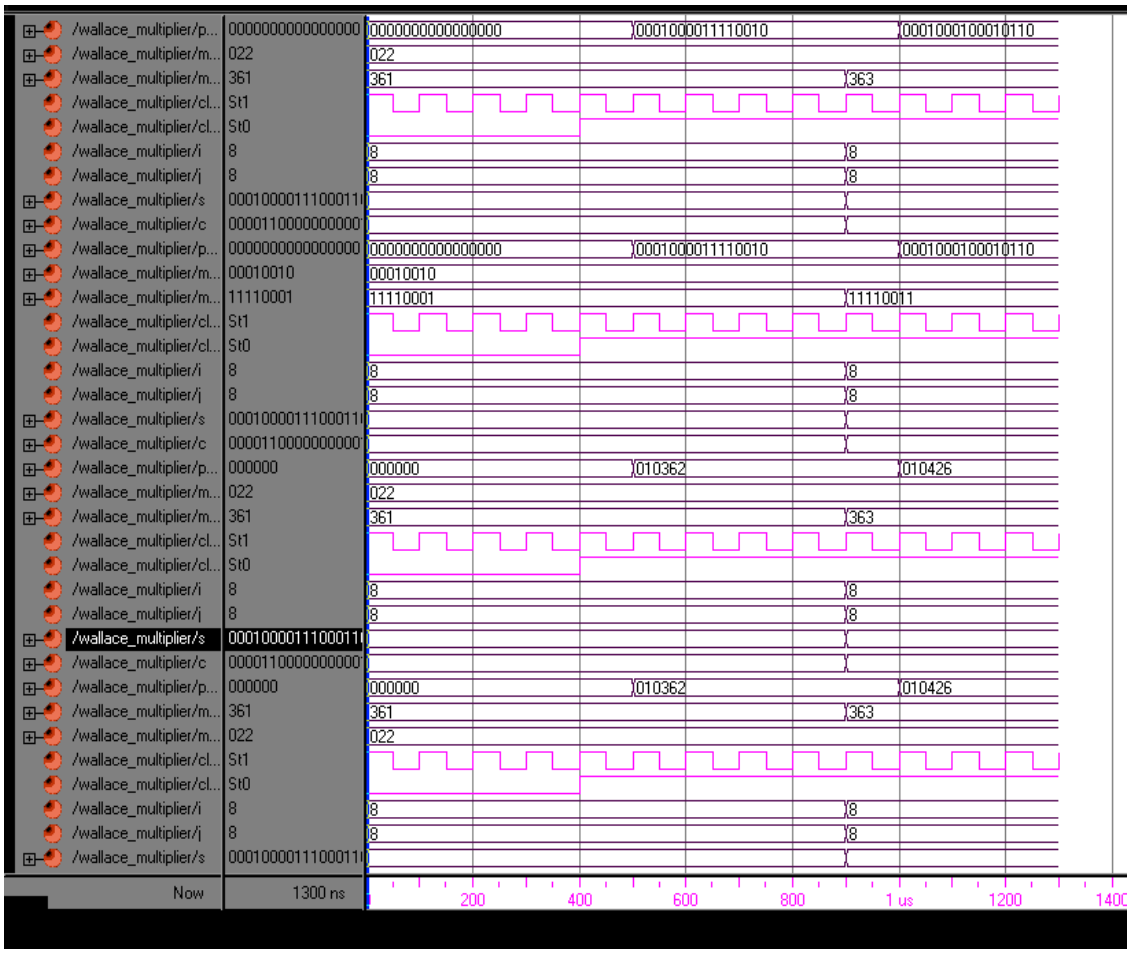


Figure 11: Simulation of **S**ingle Bit Latch Adder:

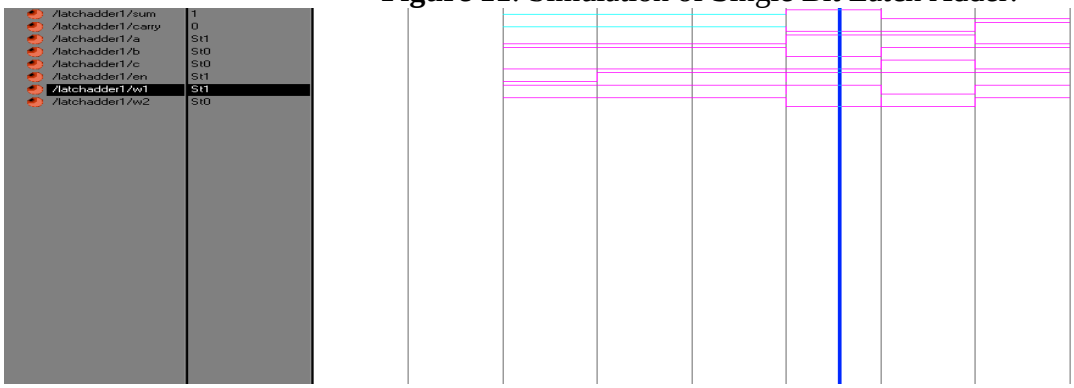
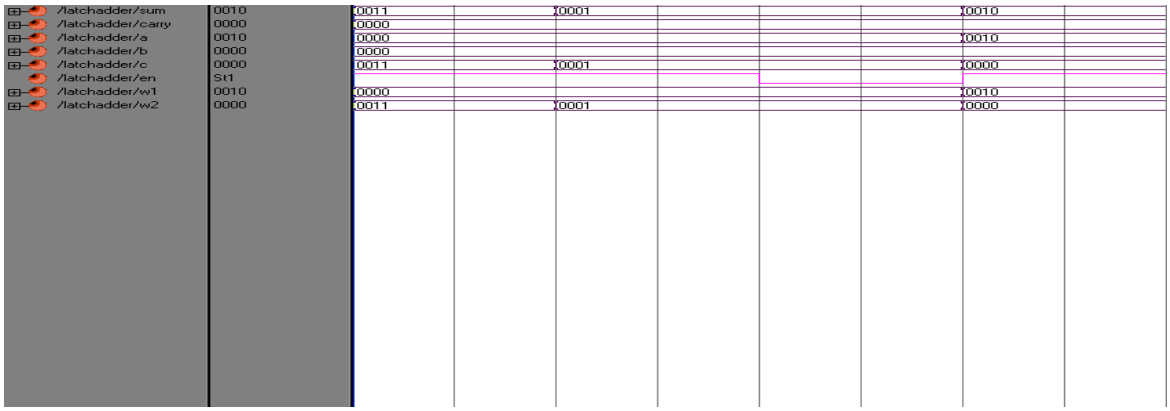


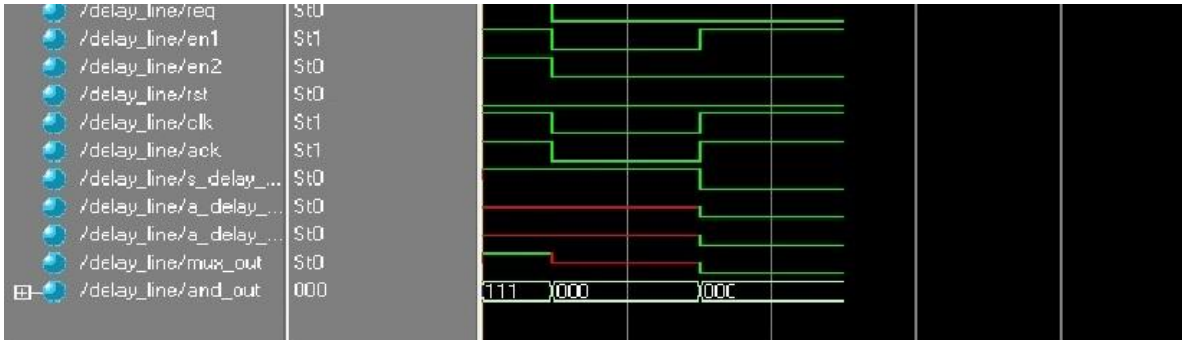
Figure 12: Simulation Result of 4 bit Latch Adder



5.7 Speculative Delay Line:

Simulation result of Speculative delay line is shown in Figure 13 .req, en1, en2, reset and clock are the inputs. And when all the above signals are enabled we get the output as 1.if any one of the signal is disabled we get the output as 0.

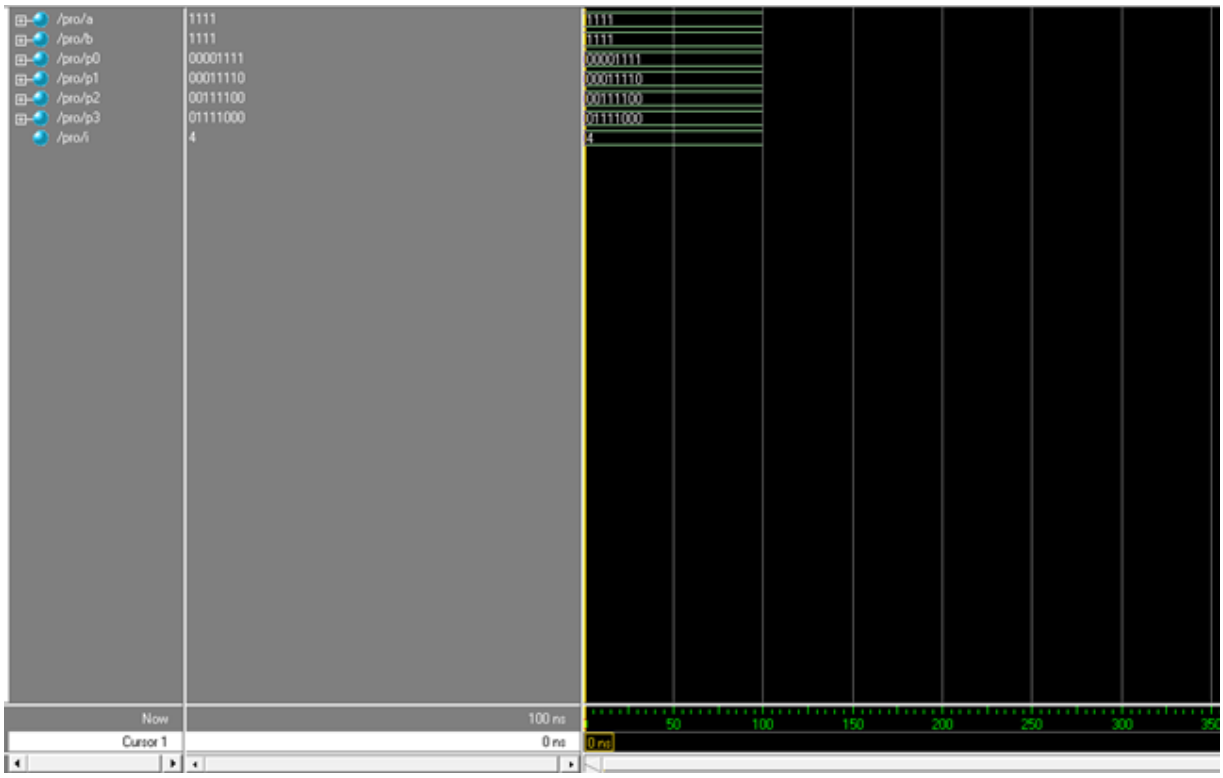
Figure 13: Simulation of Speculative Delay Line



5.8 Shift Register:

Simulation result of Shifter design is shown in Figure [14] when a is multiplicand and b is multiplier so p0,p1,p2 and p3 are the partial products.p0 we get 00001111 and in p1 it shifts one bit to the left and similarly this step takes place up to p3.

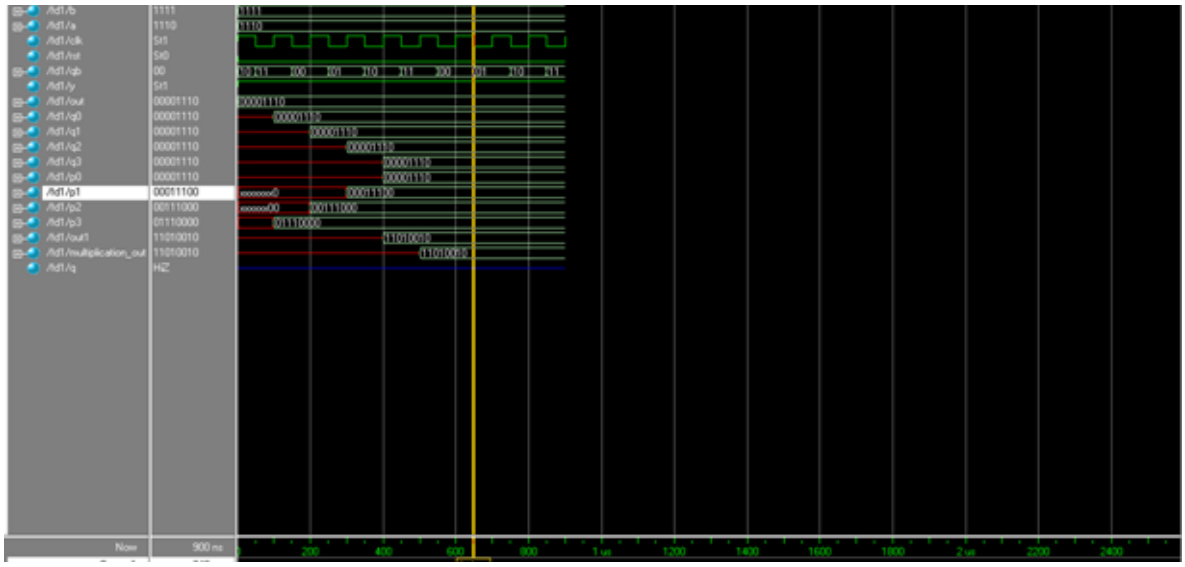
Figure 14: Simulation result of Shifter Design



5.9 Simulation Result of Synchronous Multiplier:

Simulation result of Synchronous multiplier is shown in Figure 15, a and b are the inputs out is the product.p0, p1, p2 and p3 are the partial products.

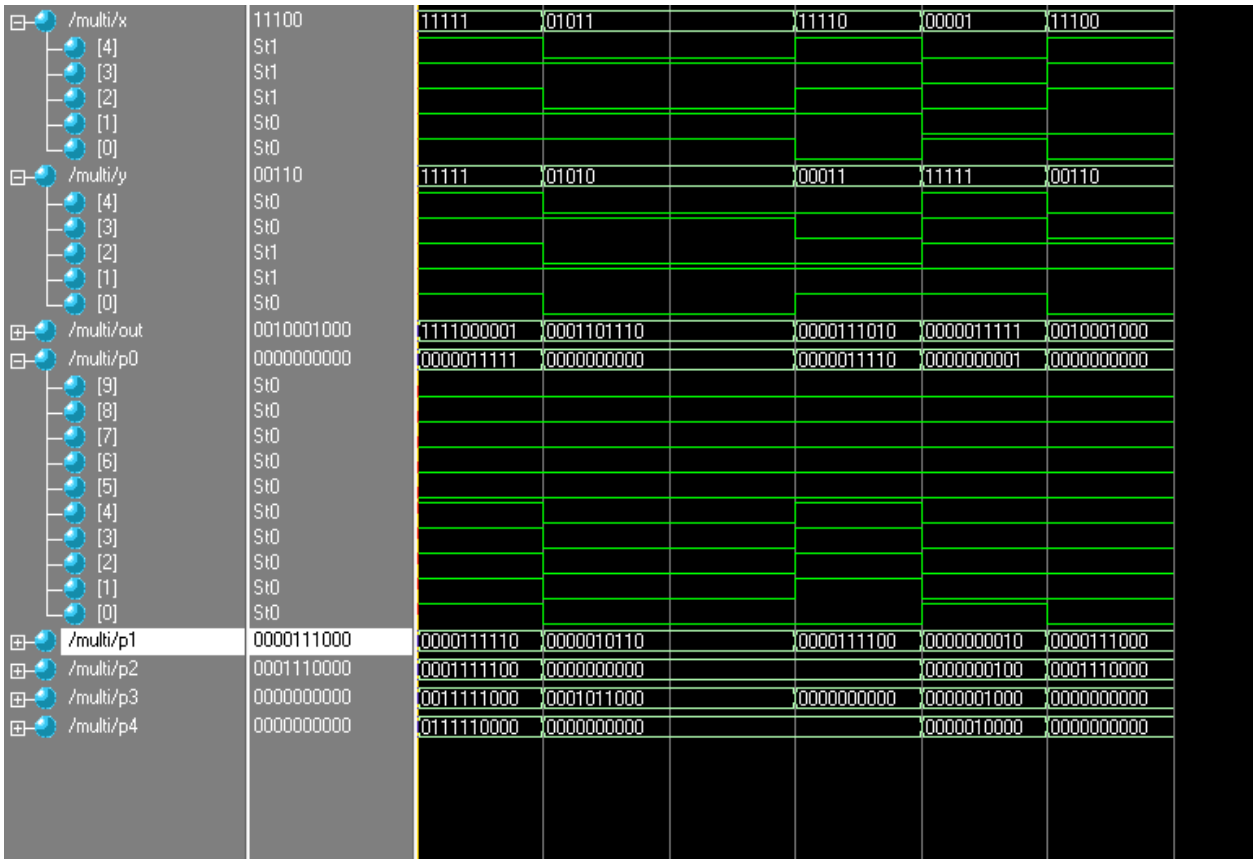
Figure 15: Simulation result of Synchronous multiplier



5.10 Simulation of Asynchronous Multiplier:

The simulation result of Asynchronous multiplier is shown in Figure 6.1. x and y are the multiplicand and multiplier. Out is the product where p0, p1, p2, p3 and p4 are the partial products in asynchronous multiplier.11100 is the input x value and 00110 is the input y value and we get the output as 0010001000.

Figure 16: Simulation result of Asynchronous multiplier



5.11 Result Comparison:

By comparing the synchronous multiplier and asynchronous multiplier, the asynchronous multiplier has low power dissipation with lesser area consumption. Because of low power dissipation and less area consumption, the FIR filter can be designed using asynchronous multiplier. The figure shows the simulation waveforms for 8 Tap FIR filter.

Table 1: Comparison table of synchronous and asynchronous Multiplier

Parameters	**Synchronous Multiplier**	**Asynchronous Multiplier**
Total Dynamic Power	76.7103 µW	65.6189 µW
Cell leakage power	157.4691 nW	156.2679 nW
Area	39.278912 μm^2	31.378545 μm^2

Figure 17: Simulated waveforms for 8 Tap FIR filter based on Asynchronous multiplier

5.12 FIR filter design simulation Results:

Table 2: FIR filter Design results

Design	Total dynamic Power(μw)	Area (μm^2)	Delay(ns)
FIR filter design using Wallace Tree multiplier	136.0156	63.278912	40.74
FIR filter design using Asynchronous multiplier	102.7441	51.378545	45.67

The simulation results shows that the Power dissipation, area and delay of the FIR filter using Wallace tree multiplier is found to be 136.0156 μw,54.278912 μm^2, 40.74ns respectively .For the proposed FIR filter design using asynchronous multiplier the power dissipation area and delay is found to be 102.7441 μw, 51.378545μm^2 and 45.67ns respectively. By comparing the existing and proposed method, power dissipation for the proposed system is reduced by 20%.

6. Conclusion

The possibility of incorporating a whole signal processing system into a chip has a multitude of effects. It will dramatically increase the processing capacity and simultaneously reduce the size of the system.

The paper is focused on the design of an efficient VLSI architecture for FIR filter which aims at reducing the hardware complexity and also to reduce the power consumption. In the existing method, Wallace tree multiplier is employed to get the better efficiency. But in Wallace tree multiplier the power is reduced compared to other types of multipliers. The main drawback is the increase in area. In order to overcome the drawback, designing of low-voltage micro power asynchronous multiplier using shift-add multiplication approach is simulated .In the proposed method the hardware complexity is reduced.

The asynchronous approach, as opposed to the prevalent synchronous approach, is an emerging design approach that potentially offers lower power dissipation and reduced area utilisation. The area is reduced in the proposed asynchronous multiplier, because the multiplier operand can be prerecorded and stored directly as control signals. The total dynamic power dissipation of FIR filter design using Synchronous multiplier is 136.0156microwatts and it is reduced to 102.7441microwatts in asynchronous multiplier based FIR filter design. Finally it is recommended that asynchronous multiplier based FIR filter design is adopted where area and power dissipation is a major concern.

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